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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/783,821	02/14/2001	Carl H. Carmichael	X-722 US	2727

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EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 03/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/783,821	CARMICHAEL ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *1* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-48* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Election/Restrictions

A telephone call was made to Justin Liu on March 8th to request an oral election to the above restriction requirement, but did not result in an election being made.

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-10 and 14-22 are drawn to a method of providing redundant logic paths containing a majority voting circuit, classified in class 326 subclass 35.

II. Claims 11-13 are drawn to a method of ensuring correct output from a logic design, classified in class 716 subclass 18.

III. Claims 23-35 are drawn to a method of maintaining configuration data using checksum values, classified in class 714 subclass 763.

IV. Claims 36-38 are drawn to a method of correcting radiation-induced errors, classified in class 365 subclass 185.32.

V. Claims 39-44 are drawn to a method of using a clock delay locked loop to correct radiation induced errors, classified in class 327 subclass 158.

VI. Claims 45-48 are drawn to a method of ensuring an FPGA device output is not erroneously asserted, classified in class 326 subclass 11.

The inventions are distinct, each from the other because:

The inventions are distinct, each from the other because of the following reasons:

Inventions Group I and Group III are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because Group I presents a circuit and method of designing a circuit providing redundant logic paths containing a majority voting circuit. Group III however presents a method of maintaining configuration data and error correction in a configurable device using checksum data. The subcombination has separate utility such as majority voting is not necessary in order to maintain configuration data and error correction in a configurable device using checksum data.

Inventions Group II and III are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention Group III has separate utility such as a method of maintaining configuration data using checksum values while Group II a method of ensuring correct output from a logic design. While

both are useable together, the method of ensuring correct output from a logic design is not necessarily required to maintain configuration data using checksums. See MPEP § 806.05(d).

Inventions Group III and Group IV are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention correcting radiation-induced errors has separate utility such as can be sued separately in communications systems without using a checksum data. See MPEP § 806.05(d).

Inventions Group V and Group III are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention Group III has separate utility such as maintaining configuration in various data storage systems such as DADS, or in computer systems. See MPEP § 806.05(d).

Inventions Group III and Group VI are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention Group VI has separate utility such as in circuits that have or require redundancy. See MPEP § 806.05(d).

Inventions Group I, a method of providing redundant logic paths containing a majority voting circuit, Group II, a method of ensuring correct output from a logic design Group III a method of maintaining configuration data using checksum values, Group IV a method of correcting radiation-induced errors. Group V a method of using a clock delay locked loop to correct radiation induced errors, and Group VI a method of ensuring a FPGA device output is not erroneously asserted are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable.

In the instant case, invention Group I has separate utility such as providing redundant logic paths containing a majority voting circuit. Invention Group II has separate utility such as ensuring correct output from a logic design. Invention Group III has separate utility such as maintaining configuration data using checksum values. Invention Group IV has separate utility such as correcting radiation-induced errors. Invention Group V has separate utility such as using a clock delay locked loop to correct radiation induced errors. Invention Group VI has separate utility such as ensuring a FPGA device output is not erroneously asserted. See MPEP § 806.05(d).

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II Group III Group IV Group V, and Group VI, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group II is not required for Group I Group III Group IV Group V, and Group VI, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group III is not required for Group I Group II Group IV Group V, and Group VI, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group IV is not required for Group I Group II Group III Group V, and Group VI, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group V is not required for Group I Group II Group III Group IV, and Group VI, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group VI is not required for Group I Group II Group III Group IV, and Group V, restriction for examination purposes as indicated is proper.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim

remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 703-308-2391. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eric J. Lamarre
for

Albert DeCady
Primary Examiner

Cynthia Britt
Examiner
Art Unit 2133